AMENDMENTS TO THE SPECIFICATION

Please replace the abstract, which begins on line 4 of page 49, with the following paragraph.

An OC-192 front-end application-specific integrated circuit (ASIC) de-interleaves an OC-192 signal to create four OC-48 signals, and decodes error-correction codes embedded in each of the four OC-48 signals. The decoder generates a Bose-Chaudhuri-Hocquenghem (BCH) error polynomial in no more than 12 clock cycles. The decoder includes several Galois field multiply accumulators, and a state machine which controls the Galois field units. ~~In the specific embodiment wherein~~ If the error-correction code is a BCH triple error-correcting code, four Galois field units are used to carry out only six equations to solve the error polynomial. The Galois field units are advantageously designed to complete a Galois field multiply/accumulate operation in a single clock cycle. The Galois field units may operate in multiply or addition pass-through modes. ~~An error insertion circuit is also provided for verifying correct operation of the BCH encoding and decoding circuits. A desired number of errors may be programmed for insertion into the OC-48 data signals. Error insertion may be performed in an iterative fashion to insert into different data signals the desired number of errors, wherein the errors are placed within the code words of the data signals at different location permutations for each data signal. In one implementation, error verification is performed using an error accumulator located in the receiver, and means are provided for examining an error accumulator count of the error accumulator to see if the number of accumulated errors matches with the number of inserted errors.~~

Please replace the paragraphs beginning on line 4 of page 1 and ending on line 17 of page 1 with the following replacement paragraphs:

The present invention is related to subject matter disclosed in the following co-pending applications, which are all hereby incorporated by reference herein in their entireties:

1. United States patent application entitled, "Error Insertion Circuit for SONET Forward Error Correction", Application Serial No. 09/821,948 ~~attorney docket no.: M-8353-US~~, naming Andrew J. Thurston and Douglas Duschatko as inventors and filed March 30, 2001 ~~substantially contemporaneously with the present application~~;

2. United States patent application entitled, "Automatic Generation of Hardware Description Language Code for Complex ~~COMPlex~~ Polynomial Functions," Application Serial No. 09/822,713 ~~attorney docket no.: M-8319-US~~, naming Andrew J. Thurston as inventor and filed March 30, 2001 ~~substantially contemporaneously with the present application~~; and

3. United States patent application entitled, "Galois Field Multiply Accumulator", Application Serial No. 09/822,733 ~~attorney docket no.: M-8341-US~~, naming Andrew J. Thurston as inventor and filed March 30, 2001 ~~substantially contemporaneously with the present application~~.

Please add the following paragraphs between lines 10 and 11 of page 10:

Figure 12 shows a state machine that controls four Galois field units, each containing a Galois field (GF) multiply accumulator (MAC).

Figure 13 shows how a "pass-through" mode, used to initialize a downstream register, is enabled.

Please replace the paragraph beginning on line 15 of page 7 and ending on line 13 of page 8 with the following replacement paragraph:

The foregoing objects are achieved in an OC-192 input/output card generally comprising four OC-48 processors and an OC-192 front-end application-specific integrated circuit (ASIC) connected to the four OC-48 processors. The OC-192 front-end ASIC has means for de-interleaving an OC-192 signal to create four OC-48 signals, and means for decoding error-correction codes embedded in each of the four OC-48 signals. The decoding means generates a Bose-Chaudhuri-Hocquenghem (BCH) error polynomial associated with a given one of the error-correction codes, in no more than 12 clock cycles. The decoding circuit includes a plurality of Galois field multiply accumulators, and a state machine which controls the Galois field units. In the specific embodiment wherein the error-correction code is a BCH triple error-correcting code, four Galois field units are used to carry out the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(x)\ (X) = 1 + S_1X$,

(4) if $(d_1 = 0)$ then $\sigma^2(x)\ (X) = \sigma^1(x)\ (X)$

else if $(d_0 = 0)$ then $\sigma^2(x)\ (X) = q_0\sigma^1(x)\ (X) + d_1X^3$

else $\sigma^2(x)\ (X) = q_0\sigma^1(x)\ (X) + d_1X^2$,

(5) $d_2 = S_5\sigma_0 + S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3$, and

(6) if $(d_2 = 0)$ then $\sigma^3(x)\ (X) = \sigma^2(x)\ (X)$

else $\sigma^3(x)\ (X) = q_1\sigma^1(x)\ (X) + d_1X^3$,

where d_i are correction factors, S_i are the BCH code syndromes, σ^i are minimum-degree polynomials, σ_i are the four coefficients for $\sigma^2(x)\ (X)$, and q_i are additional correction factors -- q_0 is equal to d_0 , unless d_0 is zero, in which case q_0 is 1, and q_i is equal to d_i, unless d_i is zero in which case $q_i=q_0$. Once the error polynomial has been generated, a

conventional technique (Chien's algorithm) can be used to search for error location numbers.

Please replace the paragraph beginning on line 6 of page 33 and ending on line 24 of page 33 with the following replacement paragraph:

This novel approach uses three correction terms d_0, d_1 and d_2 which are computed by Galois field units as discussed further below. Based on a study of the branch outcomes, error polynomial generation is reduced to the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(x)\ (X) = 1 + S_1X$,

(4) if $(d_1 = 0)$ then $\sigma^2(x)\ (X) = \sigma^1(x)\ (X)$

else if $(d_0 = 0)$ then $\sigma^2(x)\ (X) = q_0\sigma^1(x)\ (X) + d_1X^3$

else $\sigma^2(x)\ (X) = q_0\sigma^1(x)\ (X) + d_1X^2$,

(5) $d_2 = S_5\sigma_0 + S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3$, and

(6) if $(d_2 = 0)$ then $\sigma^3(x)\ (X) = \sigma^2(x)\ (X)$

else $\sigma^3(x)\ (X) = q_1\sigma^1(x)\ (X) + d_1X^3$,

where d_i are the aforementioned correction factors, S_i are the syndromes, σ^i are the minimum-degree polynomials, σ_i are the four coefficients for $\sigma^2(x)\ (X)$, and q_i are additional correction factors -- q_0 is equal to d_0 , unless d_0 is zero, in which case q_0 is 1, and q_i is equal to d_i, unless d_i is zero in which case $q_i=q_0$. The sixth syndrome is not used in the foregoing six equations, but is used when determining a "no error" condition (defined as all syndromes being equal to zero).